REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the outstanding Office Action, Claim 1 is objected to because the term "of" was missing from the phrase "selecting at least one __ the individual second...". Accordingly, applicants have amended Claim 1 to correct the apparent typographical error. Reconsideration and withdrawal of the claim objection are respectfully requested.

In addition to the above amendment to Claim 1, applicants have further amended Claim 1 to positively recite that the claimed processing steps provide a *precision element that has said target value using said desired value of said at least one of said selected elements as an offset.* Support for this amendment to Claim 1 is found throughout the specification of instant application. See, for example, paragraphs [0010], [0027], [0033], [0038] and [0041].

In addition to above amendment to Claim 1, applicants have also cancelled Claims 13-18 and have added new Claims 19-22.

New Claim 19 is derived from original Claims 1 and 2, new Claim 20 is derived from original Claim 3, new Claim 21 is derived from original Claim 4 and new Claim 22 is derived from original Claim 5. Applicants observe that new Claims 19-22 are allowable based upon the Examiner's remarks made on page 5 of the outstanding Office Action.

Since the above amendments to the claims do not introduce any new matter into the specification of the instant application, entry thereof is respectfully requested.

In the outstanding Office Action, Claims 1, 6-8, and 10-12 stand rejected under 35 U.S.C. § 102(e) as allegedly unpatentable over U.S. Patent Application Publication No. 2004/0006755 to Swanson et al. ("Swanson"). Claim 9 stands rejected under 35 U.S.C. § 103 as allegedly

unpatentable over the combined disclosures of Swanson and U.S. Patent No. 4,862,136 to Birkner ("Birkner").

Concerning the § 102(e) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that the claims of the present application are not anticipated by the disclosure of Swanson since the applied reference does not disclose applicants' claimed method recited in amended Claim 1. In particular, Swanson does not discloses the claimed processing steps which provide *a precision element that has a target value using a desired value of the at least one of the selected elements as an offset.*

Swanson provides a method to facilitate the fabrication of integrated circuits (ICs) on a wafer having a plurality of die locations comprising: measuring at least one respective parameter at a subset of the plurality of die locations on the wafer; determining at least one respective parameter for unmeasured die locations on the wafer based at least in part on at least one of the measured parameters associated with at least one of the subset of die locations; and selectively setting fuses for the plurality of die locations based on at least one of the respective parameters for the respective plurality of die locations to selectively configure ICs at each respective die location. In Swanson, one or more parameters that can affect the performance capabilities of the

ICs are first monitored at die locations. The monitored parameters are utilized to determine one or more respective parameters for unmeasured die locations, such as by interpolating parameters for measured die locations. Selective fusing can then be implemented to configure the associated ICs at die locations based on the parameters associated with respective die locations. For example, the fusing can be utilized to disconnect circuit elements (e.g., capacitors) as well as to enable circuit elements (e.g., resistors or inductors) in the ICs.

Applicants respectfully submit that the disclosure of Swanson does not provide a method of fabricating a precision element, let alone *a precision element that has a target value using a desired value of the at least one of the selected elements as an offset.*

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Swanson. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the § 103 rejection, applicants submit that the claims of the present invention are not rendered unpatentable by the disclosures of Swanson and Birkner. Specifically, the combined disclosures of Swanson and Birkner do not teach or suggest processing steps that are employed for providing a *precision element that has a target value using a desired value of the at least one of the selected elements as an offset.*

Swanson is defective for the reasons discussed above. Hence, the above remarks regarding that reference are incorporated herein by reference.

Birkner, which is applied to Claim 9, does not alleviate the defect in Swanson since the applied secondary reference also does not teach or suggest provide a method of fabricating a

precision element, let alone *a precision element that has a target value using a desired value of the at least one of the selected elements as an offset.*

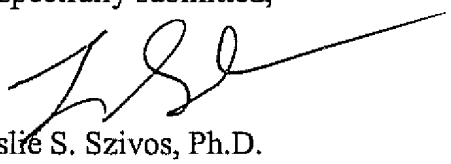
Birkner provides a programmable resistor network and a method for forming and programming the same. The network includes a plurality of independent programmable resistor arrays in a standard DIP semiconductor package. Each resistor array includes a plurality of parallel connected resistor elements capable of being selectively deleted from the array of applying a programming flow of electricity across a first and second DIP pin. The flow of electricity is of a value sufficient to progressively fuse successive array resistors. The total array resistance value progressively increases as array resistors are selectively deleted. Typically an increasing flow of electricity is applied across the array terminals until the desired array resistance value is obtained. The arrays may be manufactured in such a way that the incremental value between successive resistive elements causes the total array resistance value to increase in any desired manner, e.g., geometrically, arithmetically, and logarithmically.

The § 103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed methods to include processing steps that form the claimed precision element. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. § 103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos, Ph.D.
Registration No. 39,394

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza – Suite 300
Garden City, New York 11530
(516) 742-4343 (telephone)
(516) 742-4366 (facsimile)
LSS:vh